

Appl. No. 10/709,428
Amdt. dated February 23, 2005
Reply to Office action of December 15, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

- 1 (currently amended): A chip-packaging with bonding options connected to a package substrate, comprising:
 - a package substrate;
 - a chip mounted on the package substrate, the chip comprising a plurality of bonding pads, ~~one of the bonding pads~~ a first bonding pad being electrically connected to the package substrate without being attached to the package substrate; and
 - a lead frame connected to ~~one of the bonding pads~~ a second bonding pad.
- 2 (currently amended): The chip-packaging ~~in the of~~ claim 1, wherein the package substrate is connected to a high voltage or a low voltage.
- 3 (currently amended): The chip-packaging ~~in the of~~ claim 2, wherein the high voltage is a power supply and the low voltage is ground.
- 4 (currently amended): The chip-packaging ~~in the of~~ claim 1, wherein the lead frame is connected to a pin of the chip.
- 5 (currently amended): The chip-packaging ~~in the of~~ claim 4, wherein the pin is connected to a high voltage, a low voltage, or an input/output signal.
- 6 (currently amended): A method of packaging a chip having a bonding option connected to a package substrate, comprising:
 - providing the package substrate;

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mounting the chip on the package substrate, the chip comprising a plurality of bonding pads;
electrically connecting one of the bonding pads a first bonding pad to the package substrate without attaching the first bonding pad to the package substrate; and
connecting one of the bonding pads a second bonding pad to a lead frame.

7 (currently amended): The method of ~~packaging a chip~~ in claim 6 further comprising connecting the package substrate to a high voltage or a low voltage.

8 (currently amended): The method of ~~packaging a chip~~ in claim 7, wherein the high voltage is a power supply of the chip, and the low voltage is ground of the chip.

9 (currently amended): The method of ~~packaging a chip~~ in claim 6 further comprising connecting the lead frame to one pin of the chip.

10 (currently amended): The method of ~~packaging a chip~~ in claim 9 further comprising connecting the pin to a high voltage, a low voltage, or an input/output signal.

11 (new): A chip-packaging with bonding options connected to a package substrate, comprising:
a package substrate;
a chip mounted on the package substrate, the chip comprising a plurality of bonding pads, a first bonding pad directly contacting the package substrate; and
a first lead frame directly contacting a second bonding pad.

12 (new): The chip-packaging of claim 11, wherein the package substrate is connected to

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a high voltage or a low voltage.

13 (new): The chip-packaging of claim 12, wherein the high voltage is a power supply and the low voltage is ground.

14 (new): The chip-packaging of claim 12, wherein the first lead frame is connected to a first pin of the chip.

15 (new): The chip-packaging of claim 14, wherein the first pin is connected to a high voltage or a low voltage, the voltage level of the first pin being the logical opposite of the voltage level of the package substrate.

16 (new): The chip-packaging of claim 15, further comprising:
a second lead frame, a third bonding pad directly contacting the second lead frame.

17 (new): The chip-packaging of claim 16, wherein the second lead frame is connected to a second pin of the chip.

18 (new): The chip-packaging of claim 17, wherein the second pin is used for receiving input signals or sending output signals.

19 (new): A method of packaging a chip having a bonding option connected to a package substrate, comprising:
providing the package substrate;
mounting the chip on the package substrate, the chip comprising a plurality of bonding pads;
connecting a first bonding pad directly to the package substrate; and

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connecting a second bonding pad directly to a first lead frame.

20 (new): The method of claim 19 further comprising connecting the package substrate to a high voltage or a low voltage.

21 (new): The method of claim 20, wherein the high voltage is a power supply of the chip, and the low voltage is ground of the chip.

22 (new): The method of claim 20 further comprising connecting the first lead frame to a first pin of the chip.

23 (new): The method of claim 22 further comprising connecting the first pin to a high voltage or a low voltage, the voltage level of the first pin being the logical opposite of the voltage level of the package substrate.

24 (new): The method of claim 23, further comprising contacting a third bonding pad directly to a second lead frame.

25 (new): The method of claim 24, further comprising connecting the second lead frame to a second pin of the chip.

26 (new): The method of claim 25, wherein the second pin is used for receiving input signals or sending output signals.